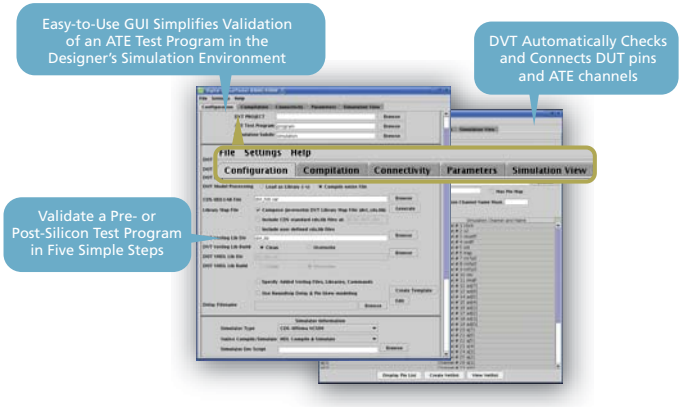
TSSI VirtualTester (TVT™) and Digital VirtualTester (DVT™)

Industry Leading Tool Cuts Pre-Silicon Debug and ATE Program Bring-Up Time in Half

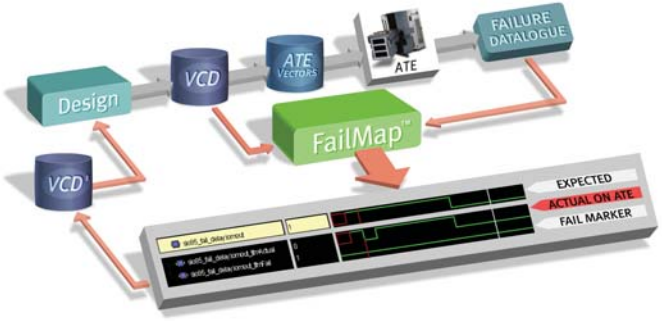


The Next-Generation Patent Pending Virtual Test Architecture

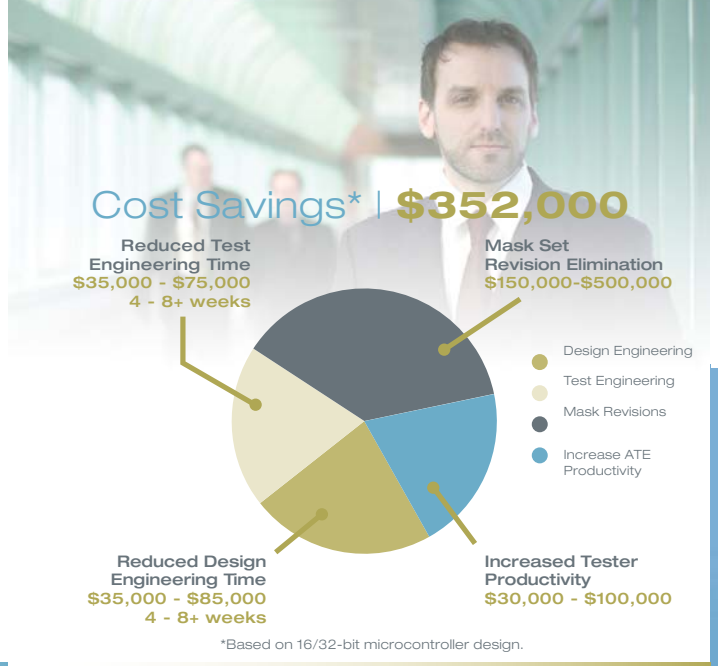
TVT FailMap™

A Design and Test Collaboration Tool

Get Composite View of Design and ATE Failure Waveforms! Mask or Fix ATE Failures Automatically!



TSSI's FailMap correlates VCD and tester's failure datalog information to create a new VCD' with 3 waveforms for each failure pin: expected, actual, and failure marker (for rapidly locating failures)



Cost Savings* | $352,000

*Based on 16/32-bit microcontroller design.

Best Returns-on-Investment

- Time-to-Volume Savings
  - 15 to 40% product cycle reduction
  - 50 to 80% less test debug time
- Typical Return-on-Investment: 5x to 10x

Most Reliable Design-to-Test Software

- Thousands of customers worldwide shave months off their projects

Innovative Company

- Invented WGL
- Patent holder of conversion and validation technologies

Global Sales and Support Network

- Experienced local teams worldwide
- Responsive Sales and Services

Full Turnkey Test Engineering Services

- Package Test and Wafer Sort
- Silicon Debug
- Digital, Mixed Signal, RF Program Development

Visit TSSI online for more details and contact information:
www.tessi.com

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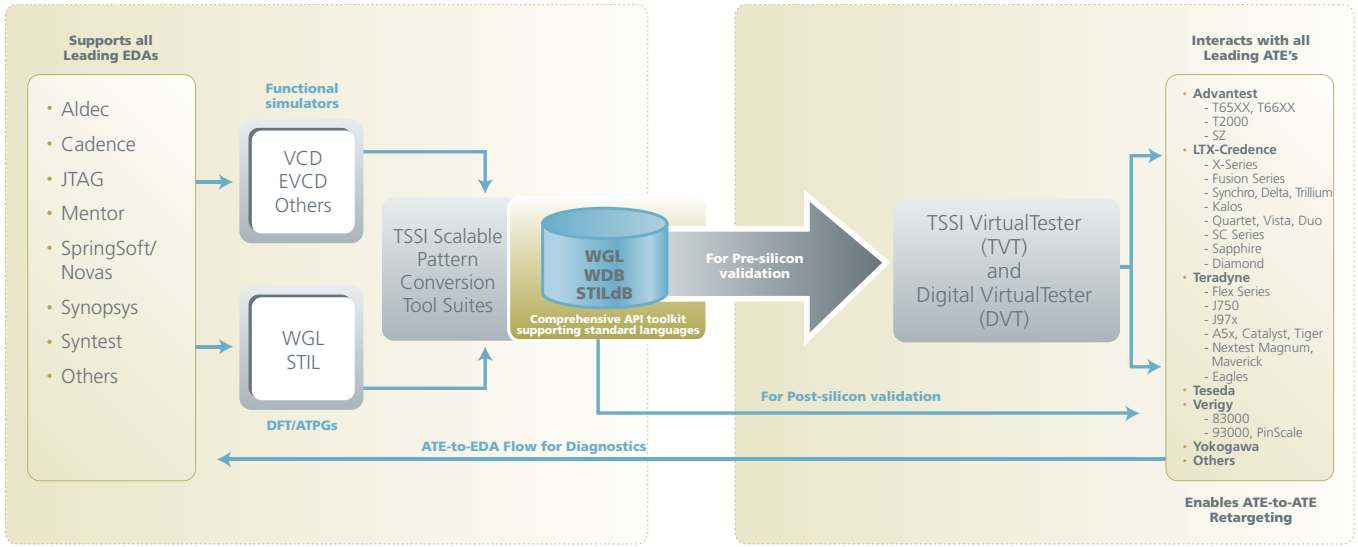
World Leading Pattern Conversion & Validation Products and Premier Test Engineering Services

EDA-to-ATE
•
DUT-on-VirtualATE
•
ATE-to-ATE
•
ATE-to-EDA
•
Digital/Mixed Signal/ RF Programming

Since 1979

Pattern Conversion

Pattern Validation



TSSI Pattern Conversion Methodologies

FEATURES

- Waveform-based Timing Analysis
- Match-and-replace exact timing specification
- External ASCII-based Tester Rules File
- Scalable Configuration from the lowest cost to the most comprehensive industrial strength tool suites
- Self-documented test development flows
- Fully customizable tool environment
- Incremental processing of hundreds of functional and scan patterns
- Reverse conversion to design testbench

BENEFITS

- Preserve designer's intent in automatic timing extraction
- Conform to exact timing spec for highest quality and reliability translation
- 100% user-controlled, user viewable rule files
- Most cost effective configuration without compromise on unforeseen test needs
- Promote team communication in natural flow-based scenarios for complex test projects
- Open environment provides 100% flexibility in tool selection
- High tool capacity handles any size of design-to-test conversion projects while producing most optimal master timing set for all patterns

TSSI Pattern Validation Methodologies

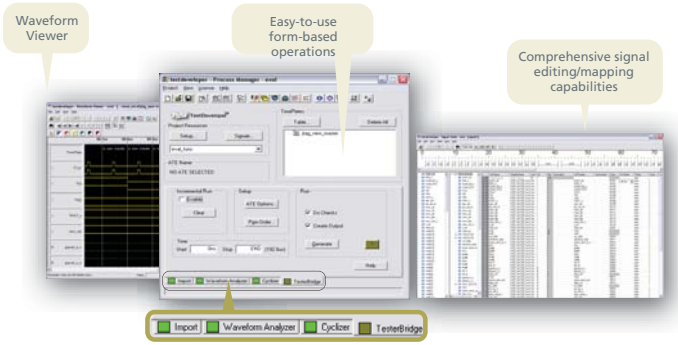
FEATURES

- Compile tester-ready programs
- Connect DUT model to Virtual ATE
- Simulate test programs in the designer's environment
- Support interaction between Verilog designs and all leading ATE models
- Workstation-based virtual test environment
- Virtual MicroProbes
- ATE-to-ATE Retargeting

BENEFITS

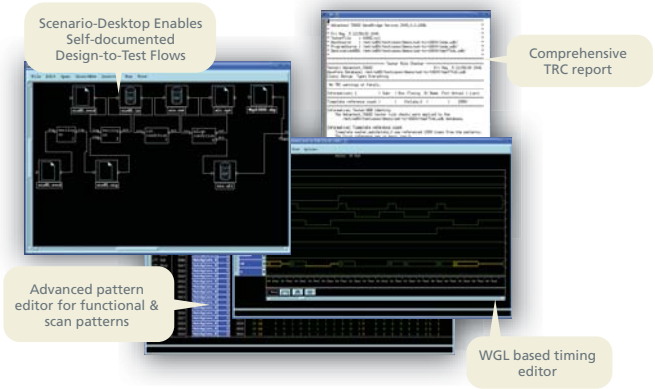
- Closed loop around the design-to-test flow without further conversion back to testbench
- Designer gets visibility of device model in the testing environment, while test engineers get a virtual debug environment before silicon
- Enable early detection of elusive timing and bus contention errors
- Save precious and costly tester time for debug of manufacturing related problems
- Debug without the access limitation of the physical environment, TSSI pattern validation tool can probe anywhere within the design or ATE model
- Reduce pattern debug and test program bring-up from months to days

TD-Scan™ & TD-Sim™ & TestDeveloper™ Easy-to-Use Low-Cost Conversion Solutions



Test Development Series (TDS™)

The De-Facto Standard Pattern Conversion Tool for More Than Two Decades



TSSI Scalable Pattern Conversion Tool Suite